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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,387	06/03/2005	Jason R Hector	Gb02 0214 US	3566
24738	7590	03/01/2007	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			NGUYEN, LAUREN	
			ART UNIT	PAPER NUMBER
			2871	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	03/01/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,387	HECTOR ET AL.	
	Examiner Lauren Nguyen	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 June 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-13 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 06/03/2005.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted was filed on the mailing date of the instant application on 06/03/2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The disclosure is objected to because of the following informalities:

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).

- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Appropriate correction is required.

Claim Objections

4. **Claim 1** is objected to because of the following informalities: the phrase 'the sets of address conductors' lacks of antecedent basis. The applicant is required to explain what is being claimed. As best understood, 'the sets of address conductors' should be –the sets of address lines--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-12** are rejected under 35 U.S.C. 102(e) as being unpatentable over **Ihara** (U.S. Patent Number 6,268,898) in view of **Song et al.** (U.S. Patent Publication 2002/0008794).

7. With respect to **claim 1**, as shown in figures 1-6, **Ihara** discloses an active matrix display device comprising first and second substrates (100 and 20), electro-optical material disposed between the first and second substrates (see at least column 1, lines 27-28), an array of display pixels (figure 2) comprising picture element electrodes (46, figure 2) and associated switches carried together with sets of address lines (41 and 42, figure 2) on the first substrate (100), and a

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common electrode (22, figure 6; see at least column 1, lines 26-27) carried on the second substrate (20), each picture element electrode (46, figure 2) together with an overlying portion of the common electrode and the electro-optical material therebetween defining a pixel, drive means (see at least column 1, lines 29-34) connected to the sets of address lines (41 and 42, figure 2) for applying drive signals to the array of pixels, the drive means comprising a drive circuit (see at least column 1, lines 29-34) which is carried on the first substrate (100) and includes conductor lines (301, 303, and 306, figure 6), the common electrode on the second substrate (22, figure 6; see at least column 1, lines 26-27) being connected electrically to at least one conductor line (306, figure 6) on the first substrate (100) that provides a drive voltage for the common electrode (see at least column 1, lines 55-60),

Ihara discloses the limitations as shown in the rejection of **claim 1** above. **Ihara** does not disclose the common electrode on the second substrate being utilised to provide electrical connection between the one conductor line and at least one other circuit element carried on the first substrate.

However, **Song et al.**, in at least paragraph 0039, lines 3-8, figures 1 and 6, discloses the common electrode (18, figure 1) being connected to at least one other circuit element (137a, figure 6) on the second substrate and **Ihara** discloses the common electrode being connected to one conductor line (306, figure 6). Therefore, the common electrode is utilised to provide electrical connection between the one conductor line and at least one other circuit element (137a, figure 6) carried on the first substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the common electrode of **Ihara** with the teaching of **Song et al.** because such

modification would improve the display characteristics of liquid crystal display devices (see at least paragraph 0025).

8. With respect to **claim 2**, as applied to **claim 1** above and shown in figures 1-6, **Ihara** discloses the drive circuit comprises at least one integrated circuit mounted on the first substrate (see at least column 2, line 15).

9. With respect to **claim 3**, as applied to **claim 1** above and shown in figures 1 and 6, **Song et al.** discloses the drive circuit comprises thin film circuit elements (137a, figure 6) integrated on the first substrate.

10. With respect to **claim 4**, as applied to **claim 1** above and shown in figures 1 and 6, **Song et al.** discloses the common electrode (18, figure 1) is connected to the at least one other circuit element (137a, figure 6) via at least one connection element (163, figure 6) extending between the first and second substrates adjacent an edge of the second substrate (see at least paragraph 0039, lines 3-8).

11. With respect to **claim 5**, as applied to **claim 1** above, **Ihara** discloses the common electrode on the second substrate (22, figure 6; see at least column 1, lines 26-27) being connected electrically to at least one conductor line (306, figure 6) on the first substrate (100).

Ihara does not disclose the remaining limitations of **claim 5**.

However, **Song et al.**, shown in figures 1-3 and 6, **Song et al.** discloses the display pixels include storage capacitors (see figure 2) which are connected at their one side to a capacitor connection line (37) carried on the first substrate (see at least paragraph 0008). **Song et al.**, in at least paragraph 0039, lines 3-8, figures 1 and 6, further discloses the common electrode (18, figure 1) being connected to at least one other circuit element (137a, figure 6) on the second

substrate. Therefore, the common electrode is utilised to provide electrical connection between the one conductor line and the capacitance connection line (137a, figure 6

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the common electrode of **Ihara** with the teaching of **Song et al.** because such modification would improve the display characteristics of liquid crystal display devices (see at least paragraph 0025).

12. With respect to **claim 6**, as applied to **claim 5** above and shown in figures 1 and 6, **Song et al.** discloses the capacitor connection line (137a) extends on the first substrate adjacent one edge of the second substrate and connects together at one side of the array a plurality of capacitor connection line row portions, each row portion being connected to the storage capacitors of a respective row of pixels, and wherein the common electrode is connected electrically with the capacitor connection line at spaced locations along that edge of the second substrate (see figure 6).

13. With respect to **claim 7**, as applied to **claim 6** above and shown in figures 1 and 6, **Song et al.** discloses the capacitor connection line (137a) also extends on the first substrate adjacent an opposing edge of the second substrate and connects together the plurality of capacitor connection row portions at the opposing side of the array (figure 6), and wherein the common electrode (18, figure 1) is connected with the capacitor connection line (137a) at spaced locations along the opposing edge of the second substrate (figure 6).

14. With respect to **claim 8**, as applied to **claim 1** above and shown in figures 1 and 6, **Song et al.** discloses the common electrode (18, figure 1) is connected to the capacitor connection line (137a) via bridging connections extending between the first and second substrates arranged along

a substantial part of the length of the edge of the second substrate (see at least paragraph 0039, lines 3-8).

15. With respect to **claim 9**, as applied to **claim 8** above and shown in figures 1 and 6, **Song et al.** discloses the bridging connections comprise conductive material disposed between the two substrates adjacent the edge of the second substrate (see at least paragraph 0039, lines 3-8).

16. With respect to **claim 10**, as applied to **claim 1** above and shown in figures 1-6, **Ihara** discloses common electrode (22, figure 6) is connected to the at least one conductive line (301, 303, and 306, figure 6) via a plurality of bridging connections (24, figure 6) arranged adjacent corners of the second substrate (27, figure 2).

17. With respect to **claim 11**, as applied to **claim 1** above and shown in figures 1-6, **Ihara** discloses the second substrate (21) carries a metallic black mask layer (23) adjacent to, and in electrical contact with, the common electrode (22, figure 6).

18. With respect to **claim 12**, as applied to **claim 1** above and shown in figures 1-6, **Ihara** discloses the electro-optical material comprises liquid crystal material (see at least column 1, lines 27-28).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimida et al. (U.S. Patent Number 5,159,477) discloses an active matrix display device having additional capacitors connected to additional capacitor common line. Komeno et al. (U.S. Patent Publication Number 2003/0063248) discloses a display device having a storage wiring pattern which is constituted of storage lines and a common line. Ichioka et al. (U.S. Patent Publication Number 2002/0171797) discloses a liquid crystal display device.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lauren Nguyen whose telephone number is (571) 270-1428. The examiner can normally be reached on M-F, 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, George Nguyen can be reached on (571) 272-4491. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lauren Nguyen

February 5, 2007

JAMES A. REAGAN
PRIMARY EXAMINER

